UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,942	03/25/2004	Nicolas Carriere	02-GR1-123	6400

23334 7590 12/30/2005

FLEIT, KAIN, GIBBONS, GUTMAN, BONGINI
& BIANCO P.L.
ONE BOCA COMMERCE CENTER
551 NORTHWEST 77TH STREET, SUITE 111
BOCA RATON, FL 33487

EXAMINER	
GHYKA, ALEXANDER G	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 12/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,942	CARRIERE ET AL.	
	Examiner	Art Unit	
	Alexander G. Ghyka	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

ALEXANDER GHYKA
PRIMARY EXAMINER
AU 2812

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claim 14 (Group II) has been cancelled. Claims 1-13 and 15-16 are now under consideration.

Claim Objections

Claims 1-13 and 15-16 are objected to because of the following informalities: Claim 1, line 7, uses the phrase "so as to completely siliciding the gate region". Appropriate correction is required, such as replacing "siliciding" with – silicide--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 5-8, 10 and 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Lim et al (US 6,271,133).

The present claims generally require a method for fabricating a transistor with a metal gate, that includes a siliciding phase comprising the formation, from a first metal, of a first metal silicide on the drain and source regions, while the gate region is protected by a layer of hard mask; removal of the hard mask; the formation, from a second metal, of a second metal silicide in the entire gate region so as to completely

silicide the gate region, while the first metal silicide is protected by the second metal; and the removal of the second metal.

Lim et al disclose a transistor having silicided regions. Lim et al disclose protecting the gate region with a hardmask **20** (Figure 4), forming a layer of TiSi2 over the source/drain region by depositing a layer of titanium and annealing with the silicon substrate **31** (Figure 5), removing hardmask layer **20** (Figure 6), and the formation of, from a second metal, of a second metal silicide in the entire gate region so as to completely silicide the gate region, while the first metal silicide is protected by the second metal; and the removal of the second metal (Figures 7-8), as required by present Claims 1, and 15-16. See column 5, lines 30-45, column 6, lines 40-65 and column 7, lines 1-25. Lim et al disclose the annealing steps as required by present Claims 2, 8 and 10. See column 7, lines 15-25 and column 8, lines 25-35. Lim et al disclose that the first metal and the second metal comprise cobalt or titanium as required by present Claims 5-6. See column 4, lines 1-20. Moreover, Lim et al disclose that the hardmask is titanium nitride as required by present Claim 7. See column 4, lines 30-35. Therefore, the present Claims are anticipated by Lim et al.

Claims 1-2, 5-6, 8, 10 and 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Sitaram et al (US 5,352,631).

The present claims generally require a method for fabricating a transistor with a metal gate, that includes a siliciding phase comprising the formation, from a first metal,

of a first metal silicide on the drain and source regions, while the gate region is protected by a layer of hard mask; removal of the hard mask; the formation, from a second metal, of a second metal silicide in the entire gate region so as to completely silicide the gate region, while the first metal silicide is protected by the second metal; and the removal of the second metal.

Sitram et al disclose a transistor having silicided regions. Sitaram et al disclose protecting the gate region with a hardmask **20** (Figure 1), forming a layer of TiSi2 over the source/drain region by depositing a layer of titanium and annealing with the silicon substrate 12 (Figure 3), removing hardmask layer **20** (Figure 4), and the formation of, from a second metal, of a second metal silicide in the entire gate region so as to completely silicide the gate region, while the first metal silicide is protected by the second metal; and the removal of the second metal (Figures 5-8), as required by present Claims 1, and 15-16. See column 4, lines 15-60, and column 5, lines 1-55 . Sitaram et al disclose the annealing steps as required by present Claims 2, 8 and 10. See column 4, lines 25-40. Lim et al disclose that the first metal and the second metal comprise cobalt or titanium as required by present Claims 5-6. See column 4, lines 15-20 and column 5, lines 45-55. Therefore, the present Claims are anticipated by Sitaram et al.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3-4, 9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim et al (US 6,271,133), as applied to claims 1-2, 5-8, 10 and 15-16 above, and further in view of Tavel et al (Totally Silicided CoSi2 Polysilicon, IEEE pgs 37.5.1-4), "Tavel et al".

Lim et al is relied upon as discussed above. Lim et al disclose the use of different metals on the source and drain and the gate regions.

Lim et al disclose the presently claimed limitations, with the exception of the formation of a cobalt silicide on both the source and drain and the gate regions.

Tavel et al disclose the formation of a silicided transistor which uses cobalt on the source, drain and gate regions and its benefit as a low gate resistivity transistors.

See page 37.5.1 and Figure 1. Tavel et al disclose temperature ranges which are encompassed by the present Claims. See 37.5.2 second column, first paragraph.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to use the same metal (cobalt) to silicide the silicided transistor of Lim et al, as disclosed by the Tavel et al reference, for its known benefit in forming a low gate resistivity transistor as disclosed by the Tavel reference. As the use of cobalt to silicide the source, drain and gate regions is known in the art as disclosed by Tavel, one of ordinary skill in the art would find it obvious to modify the Lim et al reference (which also discloses the use of cobalt) and use the same metal to silicide all three regions, for its known benefit in forming a silicided region transistor having low gate resistivity as disclosed by the Tavel et al reference. With respect to the temperature ranges as required by the present claims, where the general conditions of a claim are disclosed in the prior art, in the present case both references disclose overlapping ranges, it is not inventive to discover the optimum or workable ranges by routine experimentation. See *Allen v.* Coe 57 USPQ 136. Therefore, a *prima facie* case of obviousness is established.

Claims 3-4 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sitaram et al (US 5,352,631), as applied to claims 1-2, 5-8, 10 and 15-16 above, and further in view of Tavel et al (Totally Silicided CoSi2 Polysilicon, IEEE pgs 37.5.1-4), "Tavel et al".

Sitaram et al (US 5,352,631)et al is relied upon as discussed above. Sitaram et al (US 5,352,631) et al disclose the use of different metals on the source and drain and the gate regions.

Sitaram et al (US 5,352,631) et al disclose the presently claimed limitations, with the exception of the formation of a cobalt silicide on both the source and drain and the gate regions.

Tavel et al disclose the formation of a silicided transistor which uses cobalt on the source, drain and gate regions and its benefit as a low gate resistivity transistors. See page 37.5.1 and Figure 1. Tavel et al disclose temperature ranges which are encompassed by the present Claims. See 37.5.2 second column, first paragraph.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to use the same metal (cobalt) to silicide the silicided transistor of Sitaram et al , as disclosed by the Tavel et al reference, for its known benefit in forming a low gate resistivity transistor as disclosed by the Tavel reference. As the use of cobalt to silicide the source, drain and gate regions is known in the art as disclosed by Tavel, one of ordinary skill in the art would find it obvious to modify the Sitaram et al et al reference (which also discloses the use of cobalt) and use the same metal to silicide all three regions, for its known benefit in forming a silicided region transistor having low gate resistivity as disclosed by the Tavel et al reference. With respect to the temperature ranges as required by the present claims, where the general conditions of a claim are disclosed in the prior art, in the present case both references disclose overlapping ranges, it is not inventive to discover the optimum or workable ranges by routine

experimentation. See *Allen v.* Coe 57 USPQ 136. Therefore, a *prima facie* case of obviousness is established.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander G. Ghyka whose telephone number is (571) 272-1669. The examiner can normally be reached on Monday through Thursday during general business hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGG
December 26, 2005

ALEXANDER GHYKA
PRIMARY EXAMINER
AU 2812